Call for Papers

6th International Workshop on the Recursive InterNetwork Architecture (RINA 2019)

During the last decade research funding bodies have allocated money to fund "Future Internet" or "Clean-slate" designs that could reduce network complexity by redesigning the network protocol architecture, questioning some of its key principles. Industry groups such as the ETSI ISG NGP are looking at alternatives to the current "TCP-IP" protocol suite. However, few initiatives have really been able to "clean the slate" and question the core model and underlying principles of current Internet protocols. Of those who have done it, RINA – the Recursive InterNetwork Architecture - is probably the simplest yet most general solution.

RINA goes back to the early days of network research, in which operating systems and distributed applications were the model for thinking about packet networks. Networking was though as the enabler of distributed computing. Hence the main function of networks was to communicate applications, not devices. RINA builds on the premise that networking is Inter-Process Communication (IPC) and only IPC, to provide a theory and a model that reconstructs the overall structure of the Internet, forming a model that comprises a single repeating layer, the DIF (Distributed IPC Facility), which is the minimal set of components required to allow distributed IPC between application processes. RINA supports inherently and without the need of extra mechanisms mobility, multi-homing and Quality of Service, provides a secure and configurable environment, motivates for a more competitive marketplace and allows for a seamless adoption

We solicit papers that investigate the application of RINA in different types of network segments and applications, papers reporting on prototype implementations, experimental deployments and interoperability with existing technologies. Possible topics include but are not limited to:

- Quality of Service in RINA
- Mobility, multi-homing and multicast
- Security: authentication, access control, confidentiality
- Routing in recursive layers
- Management of recursive networks
- RINA scalability
- Policies for large-scale RINA DIFs
- Deployment scenarios for RINA
- RINA prototype implementations
- Deployment of 5G network slices enabling RINA networks
- Analysis of case studies showing benefits of RINA
- Specific RINA policies and DIF designs for wireless networks
- Specific RINA policies and DIF designs for RINA for datacentre networks
- Specific RINA policies and DIF designs for RINA for IoT networks

- Specific RINA policies and DIF designs for RINA for service provider networks
- RINA applied to Vehicular networking
- Specific RINA policies and DIF designs for RINA as a next generation virtual network overlay
- Supporting the requirements of large-scale decentralized applications (e.g. blockchains)

Submission instructions

Main track: Submitted papers must be original work, not under review at other journals/conferences, and may comprise a maximum of 6 A4 (210 mm x 297 mm) pages in 2-column IEEE conference style with a minimum font size of 10 pt. Papers should be submitted electronically using the EDAS online submission system. All accepted papers must be presented by one of the authors.

Demo track: Submitted papers must be original work, not under review at other journals/conferences, and may comprise a maximum of 4 A4 (210 mm x 297 mm) pages in 2-column IEEE conference style with a minimum font size of 10 pt. Papers should be submitted electronically using the EDAS online submission system. All accepted papers must be presented by one of the authors, who must present the demonstration at the workshop.

Important dates

- Paper submission deadline: November 22nd 2018
- Notification of acceptance: December 13th 2018
- Camera-ready due: January 10th 2019

Proceedings

Papers accepted for RINA 2019 will be included in the conference proceedings and IEEE Xplore. The IEEE reserves the right to remove any paper from IEEE Xplore if the paper is not presented at the workshop.

Workshop Co-Chairs

- Eduard Grasa (Fundació i2CAT, Spain)
- Peyman Teymoori (University of Oslo, Norway)

Technical Program Committee

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- Eduard Grasa, Fundació i2CAT, Spain
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- Ibrahim Matta, Boston University, USA
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- David Hayes, Simula Research Labs, Norway
- Giuseppe Bianchi, University of Roma Tor Vergata, Italy
- Sven van der Meer, Ericsson NM Labs, Ireland
- Yuefeng Wang, Akamai, USA
- David Hutchinson, Lancaster University, UK
- Torsten Braun, Universitat Bern, Switzerland